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@ ECE 372 – PROGRAMMING PROJECT III

@--------------------------------------------------------------------------------

@ Program implement basic application of Pulse Width Modulation in order to control

@ back light of I2C LCD by button. When pressing the button, the back light will

@ be more brightness. Program also displays my name on I2C\_LCD (New Haven 2x20)

@-------------------------------------------------------------------------------

@ Hai Dang Hoang

@ Reference: Douglas V. Hall and Leela Yadlapalli

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**.text**

**.global** \_start

**.global** INT\_DIRECTOR

**\_start:**

@----------------------------------INITIALIZE STACK---------------------------------@

LDR R13,=STACK1 @ Point to base of STACK for SVC mode

ADD R13, R13,#0X1000 @ Point to top of STACK

CPS #0x12 @ Switch to IRQ mode

LDR R13,=STACK2 @ Point to IRQ stack

CPS #0x13 @ Back to SVC mode

LDR R0,=0x4804C000 @ Base address for GPIO1 registers

ADD R4, R0,#0x190 @ Address of GPIO1\_CLEARDATAOUT register

MOV R7, #0x01E00000 @ Load value to turn off

STR R7,[R4] @ Write to GPIO1\_CLEARDATAOUT register

@---------------------------------SET UP FOR GPIO-----------------------------------@

ADD R1,R0,#0x0134 @ Get GPIO1\_OE register address

LDR R6,[R1] @ READ current GPIO1 Output Enable register

LDR R7,=0xFE1FFFFF @ Word to enable GPIO1\_21,22,23,24 as output

AND R6,R7,R6 @ Clear bit 12 (MODIFY)

STR R6, [R1] @ WRITE to GPIO1 Output Enable register

@------------------------------INITIALIZE FALLING EDGE DECTECT----------------------@

ADD R1, R0, #0x14C @ Falling edge detect

LDR R2, =0x80000000 @ Detect by GPIO1\_31

LDR R3, [R1] @ Read current value in GPIO1\_FALLING\_EDGE\_DETECT

ORR R3, R3, R2 @ Modify the current value

STR R3, [R1] @ Write modified value back to GPIO1\_FALLINGEDGEDECTECT

ADD R1, R0, #0x34 @ Get address of GPIO1\_IRQSTATUS\_SET0

STR R2, [R1] @ Enable GPIO1\_31 request on GPIO1\_IRQSTATUS\_SET0

@------------------------------Initialize INTC--------------------------------------@

@ Reset

LDR R1, =0x48200010 @ INTC\_SYSCONFIG

MOV R2,#2 @ Value for reset

STR R2,[R1] @ Software Reset

@ Enable timer interrupt

LDR R1,=0x482000C8 @ Address of INTC\_MIR\_CLEAR2 register

MOV R2, #0x10 @ Value to unmask INTC INT 68, DMTIMER2, POINTR\_PEND

STR R2, [R1] @ Write to INTC\_MIR\_CLEAR2 register

@ Enable GPIO interrupt

LDR R1,=0x482000E8 @ Address INTC\_MIR\_CLEAR3

MOV R2, #0x00000004 @ Value to unmask INTC INT 98, GPIO1, POINTRPEND1

STR R2, [R1] @ Write to INTC\_MIR\_CLEAR3 register

@ --------------------------------Initialize PWM----------------------------------@

@ Enable PWM

LDR R0,=0x44e000CC @ Address CM\_PER-EPWMSS1\_CLKCTRL

MOV R1,#0x2 @ Enable Clock for PWM

STR R1,[R0]

@ Control Module For PWM

LDR R0,=0x44e10664 @ Address of pwmss\_ctrl

MOV R1,#0x2 @ Select Timebase clock enable for PWMSS1

STR R1,[R0]

@ Pin PWM output ( Pin Mux)

LDR R0,=0x44e10848 @ Address of conf\_gpmc\_a1

MOV R1,#0x6 @ Choose Mode 6

STR R1,[R0]

@ Initial PWM

/\* Disable PWM stopping on debug events \*/

LDR R0,=0x48302200 @ Address Time-Base Control Register

LDR R1,=0xC000 @ Select Time-base Clock is divide 1

@ Select Up-count mode

@ Select Free run

STRH R1,[R0]

/\* Set period \*/

LDR R0,=0x4830220A @ Address Time-Base Period Register

LDR R1,=0xC350 @ Select Value 0xC350 for Time-base period

STRH R1,[R0]

/\* Set compare A value of the period to get duty cycle \*/

LDR R0,=0x48302212 @ Address Counter-Compare A Register

LDR R1,=0x186 @ Select 2.5% duty cycle

STRH R1,[R0]

/\* Configure output \*/

LDR R0,=0x48302216 @ Output A (EPWMxA)

MOV R1,#0x1A @ Select force EPWM xA output high

@ When counter equals active CMPA, counter increase

STRH R1,[R0]

LDR R4,=value @ R4 Register hold memory store value of duty cycle

MOV R5,#0x0 @ R5 Register is pointer control memory

@---------------------------------ENABLE CLOCK FOR I2C1-----------------------------@

LDR R0,=0x44E00048 @ Enable Clock for I2C1 (CM\_PER\_I2C1\_CLKCTRL)

MOV R1,#0x2 @ Store 2 to enable

STR R1,[R0]

@--------------------------------CONTROL MODULE I2C1--------------------------------@

LDR R8,=0x44e10958 @ use Pin 17 on P9 for SCL

MOV R9,#0x72 @ Slow slew rate/ Pull Up/ Receiver enable/ Mode 2

STR R9,[R8] @ Store

LDR R8,=0x44e1095C @ use Pin 18 on P9 for SDA

MOV R9,#0x72 @ Slow slew rate/ Pull Up/ Receiver enable/ Mode 2

STR R9,[R8] @ Store

@--------------------------------INITIAL I2C1---------------------------------------@

LDR R0,=0x4802A0A4 @ LOAD I2C\_CON Address

LDR R1,=0x0 @ Disable I2C\_EN by Storing 0

STR R1,[R0]

LDR R0,=0x4802A010 @ LOAD System Configuration Register

MOV R1,#0x0 @ Disable auto Idle

STR R1,[R0]

@ Configure Frequency = 100 KHz

@ Frequency = ICLK / ((SCLL + 7) + (SCLH + 5))

@ ICLK = 48 MHz / I2C\_PSC.PSC

@ Choose PSC = 4 --> ICLK = 48/4 = 12MHz

@ I2C\_SCLL.SCLL = I2C\_SCLH.SCLH ( Technical Reference Manual)

@ Solving SCLL = SCLH = 0x36

@ Setting PSC 3 for divide/4

LDR R0,=0x4802A0B0 @ Load I2C Clock Prescaler Register

MOV R1,#0x3 @ Divide 4

STR R1,[R0]

@ Setting SCLL and SCLH : 0x36

LDR R0,=0x4802A0B4 @ Load I2C\_SCLL Register

MOV R1,#0x36

STR R1,[R0]

LDR R0,=0x4802A0B8 @ Load I2C\_SCLH register

MOV R1,#0x36

STR R1,[R0]

LDR R0,=0x4802A094 @ Load Buffer Configuration Register

MOV R1,#0x0 @ RXTRSH/TXTRSH = 1

STR R1,[R0]

LDR R0,=0x4802A0A4 @ I2C Configuration Register

LDR R1,=0x8000 @ Enable I2C\_EN

STR R1,[R0]

@---------------------------------LCD\_INIT------------------------------------------@

LDR R0,=0x4802A028 @ Load IRQSTATUS Register

LDR R1,=0xFFFF @ Write 1 to clear all

STR R1,[R0]

@ Sending Slave address 0x3C and along with 10 data bytes

MOV R1,#0x3C @ Slave address

LDR R0,=0x4802A0AC @ Load I2C Slave Address Register

STR R1,[R0]

MOV R1,#10 @ 10 Data bytes ( Counter)

LDR R0,=0x4802A098 @ Load Data Counter Register I2C CNT

STR R1,[R0]

LDR R0,=0x4802A0A4 @ LOAD I2C\_CON Address

LDR R1,=0x8603 @ I2C Enable/Master/Transmit/STT/STP

STR R1,[R0]

@ Sending the first packet data: 0x0

MOV R1,#0x0 @ 0x0: Control Byte

BL Transmit\_Data

@ Sending the second byte data: 0x38

MOV R1,#0x38 @ 0x38: Func set

BL Transmit\_Data

@ Sending the third byte data: 0x39

MOV R1,#0x39 @ 0x39 : Func set

BL Transmit\_Data

@ Delay 10ms

BL Delay

@ Sending the fourth byte data: 0x14

MOV R1,#0x14 @ 0x14: Bias set

BL Transmit\_Data

@ Sending the fifth byte data: 0x78

MOV R1,#0x78 @ 0x78: Contrast set

BL Transmit\_Data

@ Sending the sixth byte data: 0x5E

MOV R1,#0x5E @ 0x5E: Power/ICON control/ Contrast set

BL Transmit\_Data

@ Sending the seventh byte data: 0x6D

MOV R1,#0x6D @ 0x6D: Follower control

BL Transmit\_Data

@ Sending the eighth byte data: 0x0C

MOV R1,#0x0C @ 0x0C: Display on

BL Transmit\_Data

@ Sending the ninth byte data: 0x01

MOV R1,#0x01 @ 0x01: Clear Display

BL Transmit\_Data

@ Sending the tenth byte data: 0x06 ( last data byte)

MOV R1,#0x06 @ 0x06: Entry mode set

BL Transmit\_Data

@ Wait access

BL Wait\_access

BL Turn\_off\_ardy

@ Delay 10ms

BL Delay

@--------------------------DISPLAY MY NAME------------------------------------@

LDR R0,=0x4802A028 @ Load IRQSTATUS Register

LDR R1,=0xFFFF @ Write 1 to clear all

STR R1,[R0]

@ Sending Slave address 0x3C and Data bytes

MOV R1,#0x3C @ Slave address

LDR R0,=0x4802A0AC @ Load I2C Slave Address Register

STR R1,[R0]

MOV R2,#11 @ 10 Data bytes ( Counter)

LDR R0,=0x4802A098 @ Load Data Counter Register I2C CNT

STR R1,[R0]

LDR R0,=0x4802A0A4 @ LOAD I2C\_CON Address

LDR R1,=0x8603 @ I2C Enable/Master/Transmit/STT/STP

STR R1,[R0]

@ Sending the first data: 0x80

MOV R1,#0x80 @ 0x80: Control byte

BL Transmit\_Data

@ Sending the second byte data: 0x86

MOV R1,#0x86 @ 0x86: Position

BL Transmit\_Data

@ Sending the third byte data: 0x40

MOV R1,#0x40 @ 0x40: Datasend

BL Transmit\_Data

SUB R2,R2,#3 @ Decrement counter by 3 because of sending 3 data byte

@ (0x80, 0x86, 0x40)

LDR R0,=MyName

**Display\_Name:**

@ Sending the fourth byte data: 0x48

LDRB R1,[R0],#0x1 @ Get ascii character and update pointer

BL Transmit\_Data @ Transmit data to display

SUBS R2,R2,#0x1 @ Decrement counter

BNE Display\_Name @ If decrement equal zeros --> Finish

@ Make sure processor IRQ enabled in CPSR

MRS R3, CPSR @ Copy CPSR to R3

BIC R3,#0x80 @ Clear bit 7

MSR CPSR\_c, R3 @ Write back to CPSR

**LOOP:**

NOP

B LOOP

**INT\_DIRECTOR:**

STMFD SP!,{R0-R3,LR} @ Push registers on stack

LDR R0,=0x482000F8 @ Address of INTC-PENDING\_IRQ3 register

LDR R1,[R0] @ Read INTC-PENDING\_IRQ3 register

TST R1,#0x00000004 @ TEST BIT 2

BEQ PASS\_ON @ Not from GPIOINT1A, go to back to wait loop, Else

LDR R0,=0x4804C02C @ Load GPIO1\_IRQSTATUS\_0 register address

LDR R1,[R0] @ Read Status register

TST R1,#0x80000000 @ Check if bit 31=1

BNE BUTTON\_SVC @ If bit 31=1, then button pushed

BEQ PASS\_ON @ If bit 31=0, then go to back to wait loop

**PASS\_ON:**

LDMFD SP!,{R0-R3,LR} @ Restore registers

SUBS PC,LR,#4 @ Pass execution on to wait LOOP for now

**BUTTON\_SVC:**

LDR R1,=0x80000000 @ Value to turn off GPIO1\_31 Interrupt request

@ This will turn off INTC interrupt request also

STR R1,[R0] @ Write to GPIO1\_IRQSTATUS\_0 register

@ Turn off NEWIRQA bit in INTC\_CONTROL, so processor can respond to new IRQ

LDR R0,=0x48200048 @ Address of INTC\_CONTROL register

MOV R1,#0x1 @ Value to clear bit 0

STR R1,[R0] @ Write to INTC\_CONTROL register

CMP R5,#40 @ Check Pointer is out of 40

MOVEQ R5,#0x0 @ If yes 🡪 Reset R5=0

ADDNE R5,#0x4 @ If No 🡪 Increment pointer by 4

/\* Set period again after pressing Button \*/

LDR R0,=0x48302212 @ Address Counter-Compare A Register

LDR R1,[R4,R5] @ Get value duty cycle from Memory

STRH R1,[R0] @ Store

**Done:**

LDMFD SP!,{R0-R3,LR} @ Restore registers

SUBS PC,LR,#4 @ Return from IRQ interrupt procedure

@ PROCEDURE: Transmit 1 byte data from BBB to I2C\_LCD-------------------------------@

**Transmit\_Data:**

STMFD R13!,{R0,R14} @ Store uses registers on Stack

LDR R0,=0x4802A09C @ Load I2C Data Register

STR R1,[R0] @ Store value to transmitting

@ Wait xrdy

BL Wait\_transmit

BL Turn\_off\_xrdy

LDMFD R13!,{R0,R14} @ Restore values for saved registers

MOV PC, R14 @ Return to mainline

@-----------------------------------------------------------------------------------@

@ PROCEDURE: Transmit status (XRDY) is generated when the CPU needs to put more data

@ in the I2C\_DATA register after the transmitted data has been shifted out on the SDA

@ pin. This procedure: Wait the bit XRDY before transmitting the next data byte

**Wait\_transmit:**

STMFD R13!,{R0-R1,R14} @ Store uses registers on Stack

@ Wait xrdy for transmitting

**Wait\_xrdy:**

LDR R0,=0x4802A024 @ IRQ STATUS RAW

LDR R1,[R0]

TST R1,#0x10 @ Test Bit 4

BEQ Wait\_xrdy

LDMFD R13!,{R0-R1,R14} @ Restore values for saved registers

MOV PC, R14 @ Return to mainline

@ ----------------------------------------------------------------------------------@

@ PROCEDURE: Wait\_access

@ Registers-ready-for-access (ARDY) is generated by the I2C when the previously

@ programmed address, data, and command have been performed and the status bits have

@ been updated. This bit is used to let the CPU know that the I2C registers are ready

@ for access. This procedure: Wait the bit ARDY before transmitting the next packet

**Wait\_access:**

STMFD R13!,{R0-R1,R14} @ Store uses registers on Stack

@ Wait xardy for accessing

**Wait\_ardy:**

LDR R0,=0x4802A024 @ IRQ STATUS RAW

LDR R1,[R0]

TST R1,#0x04 @ Test Bit 2

BEQ Wait\_ardy

LDMFD R13!,{R0-R1,R14} @ Restore values for saved registers

MOV PC, R14 @ Return to mainline

@-----------------------------------------------------------------------------------@

@ PROCEDURE: Turn\_off\_xrdy

@ The CPU poll this bit to write the next transmitted data into the I2C\_DATA register

@ This procedure: poll the bit XRDY

**Turn\_off\_xrdy:**

STMFD R13!,{R0-R1,R14} @ Store uses registers on Stack

LDR R0,=0x4802A028 @ Load IRQSTATUS Register

MOV R1,#0x10 @ Write 1 to clear xrdy

STR R1,[R0]

LDMFD R13!,{R0-R1,R14} @ Restore values for saved registers

MOV PC, R14 @ Return to mainline

@-----------------------------------------------------------------------------------@

@ PROCEDURE: Turn\_off\_ardy

@ The CPU poll this bit for stopping access

@ This procedure: poll the bit ARDY

**Turn\_off\_ardy:**

STMFD R13!,{R0-R1,R14} @ Store uses registers on Stack

LDR R0,=0x4802A028 @ Load IRQSTATUS Register

MOV R1,#0x4 @ Write 1 to clear ardy

STR R1,[R0]

LDMFD R13!,{R0-R1,R14} @ Restore values for saved registers

MOV PC, R14 @ Return to mainline

@-----------------------------------------------------------------------------------@

@ PROCEDURE: Delay 10ms

**Delay:**

STMFD R13!,{R0-R1,R14} @ Store uses registers on Stack

LDR R0,=0xFFFF @ Delay 10ms

**wait\_delay:**

SUBS R0,R0,#1

BNE wait\_delay

LDMFD R13!,{R0-R1,R14} @ Restore values for saved registers

MOV PC, R14 @ Return to mainline

@-----------------------------------------------------------------------------------@

**.align** 2

**SYS\_IRQ:** .WORD 0x0 @ Location to store systems IRQ address

@ Data Structure

**.data**

@ Value set for duty cycle for PWM ( Pulse Width Modulation)

**value:** **.word** 0x186, 0x30D, 0x61A, 0xC35, 0x186A, 0x30D4, 0x61A8, 0x927C, 0xAAE6, 0xB71B

**.data**

**MyName:**

**.ascii** "Hai Dang"

**STACK1:** .rept 1024

**.word** 0x0000

.endr

**STACK2:** .rept 1024

**.word** 0x0000

.endr

.END